AMENDMENTS TO THE CLAIMS

Claim 1 (currently amended): A data transmission circuit, comprising:

a first bus segment of a data bus;

a second bus segment of said data bus; and

a first switching circuit connected between said first and second segments of said data bus;[[,]]

a second switching circuit connected between said second segment of said data bus and a third segment of said data bus;

wherein

said first switching circuit is configured to selectively connect said first and second segments of said data bus such that when said first switching circuit is in a first state,

said first switching circuit passes data through from said first bus segment to said second bus segment and from said second bus segment to said first bus segment, ~~and~~

when said first switching circuit is in a second state, said second bus segment is disconnected from said first bus segment and data is passed through from said first bus segment to at least one I/O circuit and from said at least one I/O circuit to said first bus segment,[[.]]

said second switching circuit is configured to selectively connect said second and third segments of said data bus such that when said second switching circuit is

in a first state, said second switching circuit passes data through from said second bus segment to said third bus segment and from said third bus segment to said second bus segment, and

when said second switching circuit is in a second state, said third bus segment is disconnected from said second bus segment and data is passed through from said second bus segment to at least one I/O circuit and from said at least one I/O circuit to said second bus segment.

Claim 2 (canceled):

Claim 3 (currently amended): A data transmission circuit as in claim 1, [[2,]] further comprising a plurality of switching circuits each configured to selectively pass data between segments of said data bus when in said first state, and between a segment of said data bus and at least one I/O circuit when in said second state.

Claim 4 (original): A data transmission circuit as in claim 1, wherein said first switching circuit includes a two-way switch that couples said first and second bus segments when said switching circuit is in said first state, and couples said first bus segment to said at least one I/O circuit when said switching circuit is in said second state.

Claim 5 (original): A data transmission circuit as in claim 1, wherein said first switching circuit selectively connects said first and second segments of said data bus according to a selection signal received on a command and address bus.

Claim 6 (original): A data transmission circuit as in claim 1, wherein said first switching circuit selectively connects said first and second segments of said data bus according to a selection signal received on said data bus.

Claim 7 (original): A data transmission circuit as in claim 1, wherein said first switching circuit selectively connects said first and second segments of said data bus according to a selection signal received on at least one dedicated selection data path.

Claim 8 (original): A data transmission circuit as in claim 1, wherein said data bus is a multidrop bus.

Claim 9 (original): A data transmission circuit as in claim 1, wherein said data bus is a substantially stubless data bus.

Claim 10 (original): A data transmission circuit as in claim 1, wherein said first switching circuit includes a p-channel field-effect transistor (FET) switch.

Claim 11 (original): A data transmission circuit as in claim 1, wherein said first switching circuit includes a p-channel field-effect transistor (FET) switch and an n-channel FET switch.

Claim 12 (original): A data transmission circuit as in claim 1, wherein said first switching circuit is formed using Gallium Arsenide (GaAs) semiconductor technology.

Claim 13 (original): A data transmission circuit as in claim 1, wherein said first switching circuit has a programmable drive strength.

Claim 14 (original): A data transmission circuit as in claim 1, wherein said first switching circuit is located on a motherboard.

Claim 15 (original): A data transmission circuit as in claim 1, wherein said first switching circuit is located on a memory module.

Claim 16 (original): A data transmission circuit as in claim 1, wherein said first switching circuit is located on a same integrated circuit chip as a memory device.

Claim 17 (currently amended): A data transmission circuit, comprising: ~~as in claim 1,~~

a first bus segment of a data bus;

a second bus segment of said data bus; and

a first switching circuit connected between said first and second segments of said data bus,

wherein

said first switching circuit is configured to selectively connect said first and second segments of said data bus such that when said first switching circuit is in a first state, said first switching circuit passes data through from said first bus segment to said second bus segment and from said second bus segment to said first bus segment,

when said first switching circuit is in a second state, said second bus segment is disconnected from said first bus segment and data is passed through from said first bus segment to at least one I/O circuit and from said at least one I/O circuit to said first bus segment, and

when said first switching circuit receives a command selecting at least one attached I/O circuit for point-to-point communications, said first switching circuit selects said second state ~~of said first switching circuit~~ to disconnect said first bus segment from said second bus segment, and passes data between said first bus segment and said at least one attached selected I/O circuit.

Claim 18 (currently amended): A data transmission circuit, comprising: ~~as in claim 1,~~

a first bus segment of a data bus;

a second bus segment of said data bus; and

a first switching circuit connected between said first and second segments of said data bus,

wherein

said first switching circuit is configured to selectively connect said first and second segments of said data bus such that when said first switching circuit is in a first state, said first switching circuit passes data through from said first bus segment to said second bus segment and from said second bus segment to said first bus segment,

when said first switching circuit is in a second state, said second bus segment is disconnected from said first bus segment and data is passed through from said first bus segment to at least one I/O circuit and from said at least one I/O circuit to said first bus segment,

~~wherein~~ said data bus is a first data bus having a first number of data paths,

~~and~~ said first switching circuit is further configured to connect to a second data bus having a second number of data paths, and ~~wherein~~

said first switching circuit is connected between said first and second data buses for selectively receiving data on said first data bus and placing said data on said

second data bus and selectively receiving data on said second data bus and placing said data on said first data bus.

Claim 19 (original): A data transmission circuit as in claim 18, wherein said first switching circuit performs a data rate conversion between said first and second data buses.

Claim 20 (original): A data transmission circuit as in claim 19, wherein said first switching further comprises at least one of a multiplexer and demultiplexer for performing said data rate conversion.

Claim 21 (original): A data transmission circuit as in claim 18, wherein said first switching circuit further comprises at least one of a coder and decoder that performs at least one of a data encoding and decoding conversion between said first and second data buses.

Claim 22 (original): A data transmission circuit as in claim 18, wherein said first switching circuit further comprises a voltage converter that performs a voltage level conversion between said first and second data buses.

Claim 23 (original): A data transmission circuit as in claim 18, wherein said first number of data paths is less than said second number of data paths.

Claim 24 (original): A data transmission circuit as in claim 18, wherein said second data bus is connected to said at least one I/O circuit.

Claim 25 (original): A data transmission circuit as in claim 24, wherein said at least one I/O circuit includes a programmable bus terminator.

Claim 26 (original): A data transmission circuit as in claim 18, wherein said first data bus is connected to a memory controller.

Claim 27 (original): A data transmission circuit as in claim 26, wherein said memory controller includes a programmable bus terminator.

Claim 28 (original): A data transmission circuit as in claim 18, wherein said first data bus is connected to a processor.

Claim 29 (original): A data transmission circuit as in claim 18, wherein said first switching circuit is connected to said first bus segment of said first data bus via a first set of I/O pins and to said second bus segment via a second set of I/O pins.

Claim 30 (original): A data transmission circuit as in claim 29, wherein said data transmission circuit comprises a plurality of said switching circuits connected between said first and second segments of said first data bus via said first and second sets of I/O pins.

Claim 31 (original): A data transmission circuit as in claim 18, wherein said first data bus operates at a first data rate faster than a second data rate at which said second data bus operates.

Claim 32 (original): A data transmission circuit as in claim 18, wherein said first data bus operates at a first voltage level less than a second voltage level at which said second data bus operates.

Claim 33 (original): A data transmission circuit as in claim 18, wherein said first data bus transmits analog signals.

Claim 34 (original): A data transmission circuit as in claim 18, wherein said first data bus transmits digital signals.

Claim 35 (original): A data transmission circuit as in claim 18, wherein said first data bus transmits radio-frequency (RF) signals.

Claim 36 (currently amended): A data transfer interface, comprising:

a first bus segment of a data bus;

a second bus segment of said data bus; and

an interface circuit connected between said first and second segments of said data bus;[[,]]

wherein

said interface circuit includes a switching circuit configured to selectively connect said first and second segments of said data bus such that when said switching circuit is in a first state, said switching circuit passes data through from said first bus segment to said second bus segment and from said second bus segment to said first bus segment, and when said switching circuit is in a second state, said interface circuit receives and transmits data on said data bus and said second bus segment is disconnected from said first bus segment;[[.]] and

when said interface circuit receives a command selecting the interface circuit for point-to-point communications,

said interface circuit selects said second state of said switching circuit to disconnect said first bus segment from said second bus segment, and

performs at least one of receiving and transmitting data on said data bus using said first bus segment.

Claim 37 (original): An interface as in claim 36, wherein when said switching circuit is in said first state, said interface circuit does not receive or transmit data on said data bus.

Claim 38 (original): An interface as in claim 36, wherein when said switching circuit is in said second state, said interface circuit receives and transmits data using said first segment of said data bus in a point-to-point data communications configuration.

Claim 39 (original): An interface as in claim 36, wherein said switching circuit includes a field effect transistor (FET) switch.

Claim 40 (original): An interface as in claim 39, wherein said FET switch includes a p-channel transistor.

Claim 41 (original): An interface as in claim 36, wherein said switching circuit selectively connects said first and second segments of said data bus according to a selection signal received on a command and address bus.

Claim 42 (original): An interface as in claim 36, wherein said switching circuit selectively connects said first and second segments of said data bus according to a selection signal received on said data bus.

Claim 43 (original): An interface as in claim 36, wherein said switching circuit selectively connects said first and second segments of said data bus according to a selection signal received on at least one dedicated selection data path.

Claim 44 (original): An interface as in claim 36, wherein said data bus is a multidrop bus.

Claim 45 (original): An interface as in claim 36, wherein said data bus is a substantially stubless data bus.

Claim 46 (canceled):

Claim 47 (original): An data transfer interface, comprising: ~~as in claim 36,~~

a first data bus having a first number of data paths, said first data bus comprising:

a first bus segment; and

a second bus segment;

a second data bus having a second number of data paths; and

an interface circuit connected between said first segment of said data bus, said second segment of said first data bus, and said second data bus;

wherein

said interface circuit includes a switching circuit configured to selectively connect said first and second segments of said data bus such that when said switching circuit is in a first state, said switching circuit passes data through from said first bus segment to said second bus segment and from said second bus segment to said first bus segment, and when said switching circuit is in a second state, said interface circuit receives and transmits data on said data bus and said second bus segment is disconnected from said first bus segment, and

said interface circuit selectively receives data on said first data bus and places said data on said second data bus, and selectively receives data on said second data bus and places said data on said first data bus.

~~wherein said data bus is a first data bus having a first number of data paths, and further comprising a second data bus having a second number of data paths,~~

~~wherein said interface circuit is connected between said first and second data buses for selectively receiving data on said first data bus and placing said data on said second data bus and selectively receiving data on said second data bus and placing said data on said first data bus.~~

Claim 48 (original): An interface as in claim 47, wherein said interface circuit performs a data rate conversion between said first and second data buses.

Claim 49 (original): An interface as in claim 48, wherein said interface circuit further comprises at least one of a multiplexer and demultiplexer for performing said data rate conversion.

Claim 50 (original): An interface as in claim 47, wherein said interface circuit further comprises at least one of a coder and decoder that performs at least one of a data encoding and decoding conversion between said first and second data buses.

Claim 51 (original): An interface as in claim 47, wherein said interface circuit further comprises a voltage converter that performs a voltage level conversion between said first and second data buses.

Claim 52 (original): An interface as in claim 47, wherein said first number of data paths is less than said second number of data paths.

Claim 53 (original): An interface as in claim 47, wherein said second data bus is connected to at least one memory device.

Claim 54 (original): An interface as in claim 47, wherein said first data bus is connected to a memory controller.

Claim 55 (original): An interface as in claim 47, wherein said first data bus is connected to a processor.

Claim 56 (original): An interface as in claim 47, wherein said interface circuit is connected to said first bus segment of said first data bus via a first set of I/O pins and to said second bus segment via a second set of I/O pins, and I/O pins of said first set are connected to respective I/O pins of said second set through said switching circuit.

Claim 57 (original): An interface as in claim 47, wherein said first data bus operates at a first data rate faster than a second data rate at which said second data bus operates.

Claim 58 (original): An interface as in claim 47, wherein said first data bus operates at a first voltage level less than a second voltage level at which said second data bus operates.

Claim 59 (original): An interface as in claim 47, wherein said first data bus transmits analog signals.

Claim 60 (original): An interface as in claim 47, wherein said first data bus transmits digital signals.

Claim 61 (original): An interface as in claim 47, wherein said first data bus transmits radio-frequency (RF) signals.

Claim 62 (original): An interface as in claim 47, wherein said interface circuit selects data for receipt and transmission on said first data bus according to a selection signal received on a command and address bus.

Claim 63 (original): An interface as in claim 62, wherein said selection signal controls said switching circuit, whereby said first segment is disconnected from said second segment while data is being received and transmitted on said first data bus.

Claim 64 (original): A memory module, comprising:

at least one memory device; and

a data transfer interface for connection to a segmented data bus, said data transfer interface being coupled to said at least one memory device and comprising:

a first segment of said data bus;

a second segment of said data bus; and

an interface circuit configured for connection between said first and second segments of said data bus,

wherein

said interface circuit includes a switching circuit configured to selectively connect said first and second segments of said data bus such that when said switching circuit is in a first state, said switching circuit passes data through from said first bus segment to said second bus segment and from said second bus segment to said first bus segment, and when said switching circuit is in a second state, said interface circuit receives and transmits data on said data bus and said second bus segment is disconnected from said first bus segment.

Claim 65 (original): A memory system, comprising:

at least one memory device; and

a data transfer interface connected to a first segmented data bus and to said at least one memory device by a second data bus, said data transfer interface comprising:

a first segment of said first data bus;

a second segment of said first data bus; and

an interface circuit connected between said first and second segments of said first data bus,

wherein

said interface circuit includes a switching circuit configured to selectively connect said first and second segments of said first data bus such that when said switching circuit is in a first state, said switching circuit passes data through from said first bus segment to said second bus segment and from said second bus segment to said first bus segment, and when said switching circuit is in a second state, said interface circuit receives and transmits data on said first data bus and said second bus segment is disconnected from said first bus segment.

Claim 66 (original): A memory system as in claim 65, wherein said at least one memory device is included in a memory module.

Claim 67 (original): A memory system as in claim 65, wherein said switching circuit includes a field effect transistor (FET) switch.

Claim 68 (original): A memory system as in claim 67, wherein said FET switch includes a p-channel transistor.

Claim 69 (original): A memory system as in claim 65, wherein said interface circuit further comprises at least one conversion circuit which performs a data rate conversion between said first and second data buses.

Claim 70 (original): A memory system as in claim 69, wherein said at least one conversion circuit comprises at least one of a multiplexer and demultiplexer.

Claim 71 (original): A memory system as in claim 65, wherein said interface circuit further comprises a multiplexer and a demultiplexer which perform data rate conversions for data received on said first data bus that is placed on said second data bus and for data received on said second data bus that is placed on said first data bus.

Claim 72 (original): A memory system as in claim 65, wherein said interface circuit further comprises at least one of a coder and decoder that performs at least one of a data encoding and decoding conversion between said first and second data buses.

Claim 73 (original): A memory system as in claim 65, wherein said interface circuit further comprises a voltage converter that performs a voltage level conversion between said first and second data buses.

Claim 74 (original): A memory system as in claim 65, wherein said first number of data paths is less than said second number of data paths.

Claim 75 (original): A memory system as in claim 65, wherein said first data bus is connected to a memory controller.

Claim 76 (original): A memory system as in claim 65, wherein said first data bus is connected to a processor.

Claim 77 (original): A memory system as in claim 65, wherein said interface circuit is connected to said first bus segment of said first data bus via a first set of I/O pins and to said second bus segment via a second set of I/O pins, and I/O pins of said first set are connected to respective I/O pins of said second set through said switching circuit.

Claim 78 (original): A memory system as in claim 65, wherein said first data bus operates at a first data rate faster than a second data rate at which said second data bus operates.

Claim 79 (original): A memory system as in claim 65, wherein said first data bus operates at a first voltage level less than a second voltage level at which said second data bus operates.

Claim 80 (original): A memory system as in claim 65, wherein said first data bus transmits analog signals.

Claim 81 (original): A memory system as in claim 65, wherein said first data bus transmits digital signals.

Claim 82 (original): A memory system as in claim 65, wherein said first data bus transmits radio-frequency (RF) signals.

Claim 83 (original): A memory system as in claim 65, wherein said interface circuit selects data for receipt from said first data bus according to a selection signal received on a command and address bus.

Claim 84 (original): A memory system as in claim 83, wherein said selection signal controls said switching circuit, whereby said first segment is disconnected from said second segment while data is being received from said first data bus.

Claim 85 (original): A memory system as in claim 65, wherein said interface circuit is further configured to selectively receive data on said second data bus and place said data on said first data bus.

Claim 86 (original): A memory system as in claim 65, wherein said interface circuit selects data for receipt from said second data bus according to a selection signal received on a command and address bus.

Claim 87 (original): A memory system as in claim 86, wherein said selection signal controls said switching circuit, whereby said first segment is disconnected from said second segment while data is being placed on said first data bus.

Claim 88 (original): A memory system as in claim 65, wherein said first data bus is a multidrop bus.

Claim 89 (original): A memory system as in claim 65, wherein said first data bus is a substantially stubless data bus.

Claim 90 (currently amended): A data exchange system, comprising:

a data bus having a plurality of bus segments; and

a plurality of system devices each connected to said first data bus, at least one of said system devices including a switching circuit connected between first and second bus segments of said data bus for selectively passing data through from said first bus segment to said second bus segment and from said second bus segment to said first bus segment, and for selectively disconnecting said second bus segment from said first bus segment to permit point-to-point data communications between said at least one system device and another system device using one of said first and second bus segments;[[.]]

wherein a switchable terminator is included in at least one of said plurality of system devices.

Claim 91 (original): A system as in claim 90, wherein said switching circuit includes a field effect transistor (FET) switch.

Claim 92 (original): A system as in claim 91, wherein said FET switch includes a p-channel transistor.

Claim 93 (original): A system as in claim 90, wherein said plurality of system devices includes a processor.

Claim 94 (original): A system as in claim 90, wherein said plurality of system devices includes a memory controller.

Claim 95 (original): A system as in claim 90, wherein said plurality of system devices includes a bus terminator.

Claim 96 (original): A system as in claim 90, wherein said plurality of system devices includes a memory module.

Claim 97 (original): A system as in claim 90, wherein said plurality of system devices includes a memory device.

Claim 98 (original): A system as in claim 90, wherein said plurality of system devices includes an interface circuit for communication with other system devices connected to a second data bus.

Claim 99 (canceled):

Claim 100 (original): A system as in claim 90, wherein a programmable terminator is included in at least one of said plurality of system devices.

Claim 101 (original): A processor system comprising;

a processor;

at least one memory subsystem connected to said processor; and

a segmented bus which connects each of a controller and at least one memory subsystem interface circuit of said at least one memory subsystem;

whereby

said memory subsystem interface circuit couples at least one memory device to said segmented bus,

said memory subsystem interface circuit including a conversion circuit and a switching circuit, said conversion circuit receiving data from said segmented bus, converting it to data which can be processed by said at least one memory device, receiving data from said at least one memory device and converting it to data which can be transmitted over said segmented bus,

said switching circuit being connected between first and second bus segments of said segmented bus such that when said switching circuit is in a first state, said

switching circuit passes data through from said first bus segment to said second bus segment and from said second bus segment to said first bus segment, and when said switching circuit is in a second state, said interface circuit receives and transmits data on said first data bus and said second bus segment is disconnected from said first bus segment.

Claim 102 (original): A system as in claim 101, wherein said switching circuit includes a field effect transistor (FET) switch.

Claim 103 (original): A system as in claim 102, wherein said FET switch includes a p-channel transistor.

Claim 104 (original): A system as in claim 101, wherein said controller resides on a same printed circuit board as said processor.

Claim 105 (original): A system as in claim 101, wherein said controller is integrated into said processor.

Claim 106 (canceled):

Claim 107 (currently amended): A method ~~as in claim 106,~~ of data communication between devices in an electronic circuit, comprising:

connecting at least one switching circuit between segments of a data bus;

selectively passing data on said data bus through from a first bus segment to a second bus segment and from said second bus segment to said first bus segment, said selective passing of data being performed using said switching circuit, whereby when said data passing is not selected said switching circuit disconnects said first bus segment from said second bus segment to permit point-to-point data communications using one of said first and second bus segments

wherein said selective passing of data includes configuring said at least one switching circuit to pass data during WRITE operations.

Claim 108 (currently amended): A method ~~as in claim 106,~~ of data communication between devices in an electronic circuit, comprising:

connecting at least one switching circuit between segments of a data bus; and

selectively passing data on said data bus through from a first bus segment to a second bus segment and from said second bus segment to said first bus segment, said selective passing of data being performed using said switching circuit, whereby when said data passing is not selected said switching circuit disconnects said first bus segment from said second bus segment to permit point-to-point data communications using one of said first and second bus segments;

wherein said selective passing of data includes configuring said at least one switching circuit to pass data between a memory controller and a selected I/O device during READ operations.

Claim 109 (currently amended): A method ~~as in claim 106,~~ of data communication between devices in an electronic circuit, comprising:

connecting at least one switching circuit between segments of a data bus; and

selectively passing data on said data bus through from a first bus segment to a second bus segment and from said second bus segment to said first bus segment, said selective passing of data being performed using said switching circuit, whereby when said data passing is not selected said switching circuit disconnects said first bus segment from said second bus segment to permit point-to-point data communications using one of said first and second bus segments;

wherein said selective passing of data includes configuring said at least one switching circuit to pass data between a memory controller and a selected I/O device during WRITE operations.

Claim 110 (currently amended): A method of data communication between devices in an electronic circuit, comprising:

connecting a first set of I/O pins of an interface circuit to a first segment of a data bus;

connecting a second set of I/O pins of said interface circuit to a second segment of said data bus;

receiving and transmitting data on at least said first segment of said data bus using at least said first set of I/O pins; and

selectively passing data on said data bus through from said first bus segment to said second bus segment and from said second bus segment to said first bus segment, said selective passing of data being performed using a switching circuit;[[.]]

wherein when said data passing is not selected said switching circuit disconnects said first bus segment from said second bus segment to permit point-to-point data communications using one of said first and second bus segments.

Claim 111 (canceled):

Claim 112 (original): A method of data communication between devices in an electronic circuit, comprising:

connecting an interface circuit having first and second sets of I/O pins to respective first and second segments of a first data bus that operates at a first data rate;

connecting said interface circuit to a second data bus that operates at a second data rate;

receiving and transmitting data on said first data bus using said first and second sets of I/O pins;

receiving and transmitting data on said second data bus;

selectively converting data received from one of said first and second data buses for use on the other of said first and second data buses; and

selectively passing data on said first data bus through from said first bus segment to said second bus segment and from said second bus segment to said first bus segment, said selective passing of data being performed using a switching circuit, whereby when said data passing is not selected said switching circuit disconnects said first bus segment from said second bus segment to permit point-to-point data communications using one of said first and second bus segments.

Claim 113 (original): A method as in claim 112, wherein said selectively converting data includes using a selection signal to determine whether to convert for use on the other of said first and second data buses.

Claim 114 (original): A method as in claim 113, wherein said selective conversion of data is performed when said interface circuit is selected for operation by said selection signal.

Claim 115 (original): A method as in claim 113, wherein said selective conversion of data is not performed when said interface circuit is not selected for operation by said selection signal.

Claim 116 (original): A method as in claim 112, wherein said first data rate is faster than said second data rate.

Claim 117 (original): A method as in claim 112, further comprising converting received data between said first data rate of said first data bus and said second data rate of said second data bus.

Claim 118 (original): A method as in claim 112, further comprising converting received data between a first encoding of said first data bus and a second encoding of said second data bus.

Claim 119 (original): A method as in claim 112, further comprising converting received data between a first voltage level of said first data bus to a second voltage level of said second data bus.

Claim 120 (original): A method as in claim 119, wherein said first voltage level is less than said second voltage level.

Claim 121 (original): A method as in claim 112, wherein said first data bus connects to said first and second sets of I/O pins using a first bus width different from a second bus width used to connect said interface circuit to said second data bus.

Claim 122 (original): A method as in claim 121, wherein said first bus width is less than said second bus width.

Claim 123 (original): A method as in claim 112, wherein devices of a first technology communicate with said interface circuit using said first data bus and devices of a second technology communicate with said interface circuit using said second data bus.

Claim 124 (original): A method as in claim 123, wherein said devices of said first technology include at least one processor.

Claim 125 (original): A method as in claim 123, wherein said devices of said second technology include at least one memory device.

Claim 126 (original): A method as in claim 112, wherein said first data bus is a multi-drop bus.

Claim 127 (original): A method as in claim 112, wherein said first data bus is a substantially stubless data bus.